AMENDMENTS TO THE CLAIMS

Kindly amend claims 1, 6, 9-11, and 19-23 as shown in the following listing of claims. The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) An integrated circuit (IC), comprising:

a plurality of skew-programmable clock buffers, each receiving a distributed clock signal and providing a corresponding one of a plurality of local clock signals each having a programmed skew;

~~fixed skew logic~~fixed skew logic circuit that enables permanent programming of a plurality of static skew values;

an external interface that enables programming of a plurality of dynamic skew values; and

a skew controller, coupled to said external interface, to said plurality of skew-programmable clock buffers, and to said ~~fixed skew logic~~fixed skew logic circuit, that selects between said dynamic skew values and said static skew values and that programs each of said plurality of skew-programmable clock buffers based on selected skew values.

2. (Original) The IC of claim 1, wherein said skew controller is operative to detect a skew over-ride command upon reset of the IC, to select said dynamic skew values programmed into a programmable memory if said skew over-ride command is detected, and to select said plurality of static skew values if said skew over-ride command is not detected.

3. (Original) The IC of claim 2, wherein said programmable memory is integrated on the IC.

4. (Original) The IC of claim 2, wherein said programmable memory is externally coupled via said external interface.

5. (Original) The IC of claim 1, wherein said skew controller outputs a serial stream of binary encoded bits.

6. (Currently Amended) The IC of claim 5, wherein each of said plurality of skew-programmable clock buffers comprises:

   ~~delay-intercept logic~~delay intercept logic circuit, coupled to said skew controller, that intercepts selected ones of said binary encoded bits and that outputs at least one corresponding set of delay bits; and

   at least one local clock buffer, each said local clock buffer receiving said distributed clock signal and a corresponding set of delay bits and providing a corresponding one of said plurality of local clock signals having a skew determined by said corresponding set of delay bits.

7. (Original) The IC of claim 6, wherein each said local clock buffer comprises:

   a plurality of sequentially-coupled buffers having an input receiving said distributed clock signal, at least one intermediate node, and an output providing a corresponding one of said plurality of local clock signals; and

   at least one array of P-channel and N-channel devices, each said array having a plurality of inputs receiving said corresponding set of delay bits and at least one output coupled to said at least one intermediate node.

8. (Original) The IC of claim 7, wherein each said array of P-channel and N-channel devices comprises an N-channel array including a plurality of binarily-distributed N-channel devices with floating sources having inputs receiving true encoded delay bits from said corresponding set of delay bits and having an output coupled to said intermediate node, and a P-channel array including a plurality of binarily-distributed P-channel devices with floating sources having a plurality of inputs receiving complementary encoded delay bits from said corresponding set of delay bits and having an output coupled to said intermediate node.

9. (Currently Amended) The IC of claim 1, wherein said ~~fixed-skew logic~~fixed skew logic circuit comprises a plurality of fuses.

10. (Currently Amended) The IC of claim 1, wherein said a ~~fixed skew logic~~fixed skew logic circuit comprises an electrically programmable read-only memory.

11. (Currently Amended) A method of tuning clock skews for an integrated circuit (IC), comprising:

determining, by the IC upon reset, whether a skew over-ride command is provided;

selecting skew values from a ~~fixed skew logic~~fixed skew logic circuit integrated on the IC if the skew over-ride command is not provided;

selecting skew values from a skew memory if the skew over-ride command is provided;

programming at least one programmable delay block integrated on the IC based on selected skew values; and

receiving, by each delay block, a distributed clock signal and providing at least one local clock signal having a skew based on a selected skew value.

12. (Original) The method of claim 11, wherein said programming at least one programmable delay block comprises:

providing a serial stream of binary encoded delay bits;

intercepting the serial stream and selecting corresponding ones of the binary encoded delay bits; and

providing selected true and complementary binary encoded delay bits.

13. (Original) The method of claim 12, further comprising:

providing selected true binary encoded delay bits to gates of at least one binarily-distributed array of N-channel devices with floating sources integrated on the IC;

providing selected complementary binary encoded delay bits to gates of at least one binarily-distributed array of P-channel devices with floating sources integrated on the IC; and delaying a distributed clock signal through a plurality of sequentially-coupled clock buffers coupled to corresponding arrays of N-channel and P-channel devices.

14. (Original) The method of claim 11, further comprising:

integrating the skew memory as a dynamic memory on the IC; and

programming the skew memory via an external interface.

15. (Original) The method of claim 14, further comprising:

programming a skew over-ride bit in the skew memory; and

said determining whether a skew over-ride command is provided comprising reading the skew over-ride bit.

16. (Original) The method of claim 15, further comprising holding the IC in reset during said programming the skew memory and said programming a skew over-ride bit.

17. (Original) The method of claim 11, wherein said selecting skew values from the skew memory comprises reading the skew memory coupled to the IC via an external interface.

18. (Original) The method of claim 17, wherein said determining whether a skew over-ride command is provided comprises monitoring the external interface.

19. (Currently Amended) The method of claim 11, further comprising:

programming the skew memory with dynamic skew values and providing the skew over-ride command during reset of the IC;

testing the IC programmed with the dynamic skew values;

repeating said programming and testing to determine an optimum set of skew values; and

programming the ~~fixed skew logic~~fixed skew logic circuit with the optimum set of skew values.

20. (Currently Amended) The method of claim 19, wherein said programming the ~~fixed skew logic~~fixed skew logic circuit comprises blowing at least one fuse integrated on the IC via laser.

21. (Currently Amended) The method of claim 19, wherein said programming the ~~fixed skew logic~~fixed skew logic circuit comprises programming an electrically programmable read-only memory integrated on the IC.

22. (Currently Amended) A system for fine tuning clock signals of an IC, comprising:

a permanent programmable block for permanently programming at least one fixed skew value;

~~programmable logic~~programmable logic circuit for storing at least one dynamic skew value;

at least one clock buffer, each including programmable delay logic that delays a clock signal based on a selected skew value; and

a skew controller, coupled to said permanent programmable block, said ~~programmable logic~~programmable logic circuit and said at least one clock buffer, that selects between said at least one fixed skew value and said at least one dynamic skew value and that programs said at least one clock buffer using the selected skew value.

23. (Currently Amended) The system of claim 22, wherein said ~~programmable logic~~programmable logic circuit is incorporated on the IC and programmed via an external interface.

24. (Original) The system of claim 22, wherein said at least one clock buffer comprises at least one buffer coupled to an array of binarily-distributed N-channel devices and P-channel devices.

25. (Original) The system of claim 24, where said array comprises P-channel and N-channel device pairs that are matched to provide substantially the same resistive/capacitive characteristics.

26. (Original) The system of claim 22, wherein said skew controller reads at least one skew over-ride bit programmed on the IC to select between said at least one fixed skew value and said at least one dynamic skew value.